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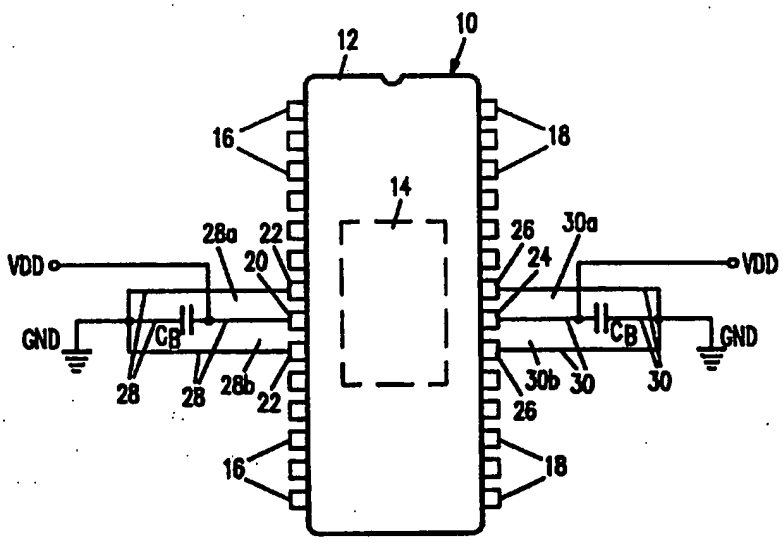

(57) Abstract

A packaged integrated circuit ("IC") with reduced radiation of and susceptibility to electromagnetic fields includes three pins for power supply (e.g. VDD or VCC) and ground connections among a group of signal pins along a side of the IC package. In one embodiment, the power supply connection uses one pin while the ground connection uses the two adjacent pins on either side thereof. In another embodiment, the ground connection uses one pin while the power supply connection uses the two adjacent pins on either side thereof. Within the IC, the power supply and circuit ground conductors integrated therein form a supply current loop and a return current loop, respectively, which are closely spaced, and substantially symmetrical and coplanar. The directions of flow of the supply currents and return currents oppose each other, thereby creating opposing and substantially self-cancelling electromagnetic fields.

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PACKAGED INTEGRATED CIRCUIT WITH REDUCED ELECTROMAGNETIC INTERFERENCE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to packaged integrated circuits, and in particular, packaged integrated circuits with pin assignments selected to reduce electromagnetic interference.

2. Description of the Related Art

As the operating speeds of modern digital integrated circuits ("ICs") increases, so do their signal state switching speeds. In other words, the digital ICs of today operate increasingly faster with higher clocking rates and faster signal state slew rates, i.e. faster signal state rise and fall times. A byproduct of this is increased radiation of electromagnetic fields.

The majority of the electromagnetic fields radiated from a packaged IC, as well as most of the sensitivity of a packaged IC to electromagnetic fields, comes from the conductive circuit loop formed between the power supply and circuit ground. This conductive loop consists primarily of the conductive power supply path formed within the IC itself (i.e. the power supply and ground conductors integrated therein), the IC package pins, the bond wires connecting the IC to the IC package pins, the conductive traces of the printed circuit board upon which the packaged IC is mounted, and an external power supply bypass capacitor.

Through this loop, the switching current flows (e.g. dc and low frequency components from the power supply and high frequency components from the external, precharged, bypass capacitor) through the IC to circuit ground, thus generating an electromagnetic field with many frequency components, the higher of which in particular are radiated. It is this same conductive loop into which externally generated electromagnetic fields can induce current, thereby potentially inducing changes in the instantaneous power supply voltage on board the IC, which in turn, can cause spurious changes in logic state levels.

One technique which has been used to reduce such radiation of and susceptibility to electromagnetic fields involves the use of external shielding. Examples of such shielding include metal enclosures and extensive ground plane surrounding the offending (or sensitive) IC. However, such external shielding adds complexity and costs, particularly for fabrication, testing and assembly.

Another technique which has been used involves the placement of the power supply connection, i.e. the packaged IC pin to which the power supply is connected, in (or near) the center of a group of signal pins along one side of the packaged IC. Further discussion of this technique can be found in M. Polacek, M. Coenen and W. Rosink, "Electromagnetic Compatibility of ACL: Comparison Between Corner and Center Supply Pinned Octal Drivers, Theory and Tests", Wescon/89 Conference Record, November 14–15, 1989, pp. 113–118, the disclosure of which is incorporated herein by reference. While this technique can reduce such radiation of and susceptibility to electromagnetic fields to some extent, with increasingly faster switching speeds in modern digital ICs, even further improvement would be desirable.

SUMMARY OF THE INVENTION

A packaged IC with reduced radiation of and susceptibility to electromagnetic fields in accordance with a preferred embodiment of the present invention includes an IC package within which is an IC which includes a power supply conductor, a ground conductor and multiple signal conductors therein. Multiple signal connectors (e.g. pins) are disposed along an edge of the IC package and are connected (e.g. via

bond wires) to a number of the signal conductors within the IC. Also disposed along that edge of the IC package and among the multiple signal connectors are at least three connectors (e.g. pins) which are connected to the IC power supply conductor and ground conductor within the IC.

In a preferred embodiment of the present invention, one of the three connectors is connected to the IC power supply conductor, while the adjacent connectors on either side thereof are connected to the IC ground conductor. In an alternative preferred embodiment of the present invention, one of the three connectors is connected to the IC ground conductor, while the adjacent connectors on either side thereof are connected to the IC power supply conductor.

In a further alternative preferred embodiment of the present invention, power supply and ground connectors in accordance with the above-described configurations are disposed along two edges (e.g. opposing edges) of the IC package.

These and other features and advantages of the present invention will be understood upon consideration of the following detailed description of the invention and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A, 1B and 1C illustrate a packaged IC using a dual in-line pin package in accordance with the present invention.

Figures 2A, 2B and 2C illustrate a packaged IC using a flat-pack package in accordance with the present invention.

Figures 3, 4, 5 and 6 illustrate internal power supply and ground conductors and connections for packaged ICs in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Figure 1A, a packaged IC 10 in accordance with a preferred embodiment of the present invention includes a dual in-line package ("DIP") IC package 12 within which an IC 14 is enclosed in accordance with well known techniques. Disposed along opposing edges, or sides, of this DIP IC package 12 are groups 16, 18 of signal connectors, e.g. pins. Along one side of the package 12, among the signal connectors 16, is a power supply connector (i.e. pin) 20 to which is applied a power supply voltage VDD for powering the IC 14. On either side of and adjacent to this power supply connector 20 are two ground connectors (e.g. pins) 22 which are connected to circuit ground GND for providing a circuit ground for the IC 14. Connected between the power supply VDD and circuit ground GND is a bypass capacitor C_B. (As is well known in the art, bypass, or decoupling, capacitors, typically having small values of capacitance on the order of 0.01 microfarad or less and electrically connected closely to the power supply connection to be decoupled, help to reduce emissions of and susceptibility to electromagnetic fields.)

Along the opposing edge, or side, of the package 12, among the other signal connectors 18, another power supply connector 24 can also be used to provide the power supply voltage VDD to the IC 14. Again, on either side of and adjacent to this connector 24 are two ground connectors 26 for providing another circuit ground GND connection for the IC 14. As with the power supply VDD connector 20 on the other side of the package 12, a decoupling capacitor C_B is electrically connected across the power supply connector 24 and ground connectors 26 for decoupling this power supply voltage VDD connector 24.

With respect to radiation of and susceptibility to electromagnetic fields, the frequency range of primary interest is one megahertz (1 MHz) through one gigahertz (1 GHz). For this frequency range, the approximate wavelengths ("λ") range from 300 meters to 30 centimeters. For ICs, the dimensions of the

current loop of concern for this frequency range is formed by the connection at the power supply pin, circuit ground pin and bypass capacitor C_B and is approximately one centimeter (1 cm). Accordingly, the diameter of the current loop is less than or equal to one-thirtieth of a wavelength ($\leq\lambda/30$) in length. Therefore, radiation of or susceptibility to electromagnetic fields is directly proportional to the area of the current loop.

If substantially identical current loops are placed tangent to one another within the same plane, with their loop centers separated by a distance equal to their diameters, where the diameter is less than one-thirtieth of a wavelength ($<\lambda/30$), and the currents within the loops are of equal magnitude but opposite in direction of current flow (e.g. one clockwise and another counterclockwise), then the far field strength radiating from the combination of the two current loops will be greatly reduced, e.g. to less than one-thirtieth (<1/30) of that if only one current loop were present.

Accordingly, the current loops 28a and 28b formed by the power supply VDD and ground GND circuit connections 28 and decoupling capacitor C_B are configured to be substantially symmetrical and coplanar. That, with the conduction of equal and opposite currents due to the above-described three-connector power supply and ground connections, results in reduced radiation of and susceptibility to electromagnetic fields. Similarly for the other side of the IC package 12, the current loops 30a and 30b formed by the power supply VDD and ground GND connections 30 and decoupling capacitor C_B are configured to be substantially symmetrical and coplanar.

Referring to Figure 1B, similar results can be obtained by using single connectors 21, 25 for the circuit ground GND and two adjacent connectors 23, 27 on either side thereof for the power supply VDD connection. As for the embodiment of Figure 1A, the current loops 29a and 29b, and 31a and 31b, are configured to be substantially symmetrical and coplanar.

Referring to Figure 1C, it can be seen that with a typical DIP IC package having a pin spacing 32 of approximately 0.1 inch, 0.05 inch (small outline package ["SOP"]) or 0.025 inch (shrink small outline package ["SSOP"]), the desired current loop diameter, i.e. $<\lambda/30$, can be easily achieved, particularly with surface mount components such as monolithic chip capacitors for the bypass capacitors C_B.

Referring to Figure 2A, a packaged IC 110 in accordance with another preferred embodiment of the present invention includes a flat package 112 (e.g. plastic quad flat package ["PQFP"] or plastic leaded chip carrier ["PLCC"]) within which an IC 114 is enclosed in accordance with well known techniques. Along one edge, or side, of the package 112 are disposed a number of signal connectors (e.g. pins) 116. Along an opposing edge are a number of additional signal connectors 118, while along adjacent edges therebetween are further signal connectors 117, 119.

Similar to the packaged IC 10 of Figure 1A, one connector 120 is used to provide connection to a power supply VDD, while adjacent connectors 122 on either side thereof provide connections to circuit ground GND for the IC 114. In accordance with the foregoing discussion, the current loops 128a and 128b (formed by the connections 128 between the connectors 120, 122 and the power supply VDD, circuit ground GND and decoupling capacitor C_B) are configured to be substantially symmetrical and coplanar.

Similarly, along the opposing edge of the package 112, a connector 124 and adjacent connectors 126 can be used for providing connections to the power supply VDD and circuit ground GND, respectively, for the IC 114. The current loops 130a and 130b (formed by the connections 130 between these connectors 124, 126 and the power supply VDD, circuit ground GND and decoupling capacitor C_B) are substantially symmetrical and coplanar.

Referring to Figure 2B, a similar packaged IC 111 can be constructed in accordance with the present invention by using single connectors 121, 125 for the circuit ground GND connection, with adjacent connectors 123, 127 for providing the power supply VDD connections. As with the packaged IC 110 of Figure 2A (and those of Figures 1A and 1B), the power supply current loops 129a and 129b, and 131a

and 131b, formed by the connections 129 and 131 between the connectors 121 and 123, and 125 and 127, respectively, and the power supply VDD, circuit ground GND and decoupling capacitor C_B, are designed to be substantially symmetrical and coplanar.

Referring to Figure 2C, it can be appreciated that with this flat-pack IC package 112 design, with a typical pin spacing 132 of approximately 0.05 inch (PLCC) or 0.025 inch (PQFP), the above-discussed desired loop dimension of $<\lambda/30$ can be easily achieved, particularly with surface mount components such as monolithic chip capacitors for the bypass capacitors C_B.

Figures 3 through 6 and the following discussion illustrate how the power supply VDD and ground GND conductors integrated within the IC 114 of Figure 2 can be configured to support the symmetrical three-connector power supply VDD and ground GND connections, which in turn, support the external symmetrical current loop configurations 128a and 128b, 130a and 130b (Figure 2A), 129a and 129b, and 131a and 131b (Figure 2B). It should be understood, however, that Figures 3 through 6 and the following discussion have similar application to the ICs 14 of Figures 1A and 1B.

Referring to Figure 3, an IC 114a having an integrated power supply VDD 220 and ground GND 222 conductor configuration suitable for the power supply 120 and ground 122 connectors configuration along one edge of the packaged IC 110 (Figure 2A) can be designed as shown. Signal conductors 116a, 117a, 118a, 119a surround the active chip area, with power supply 120a and ground 122a conductors disposed among them as shown. A bonding wire 120b connects the power supply conductor 120a to the power supply connector 120, while additional bonding wires 122b connect the ground conductors 122a to the ground connectors 122.

In this IC design 114a, the power supply VDD 220 and ground GND 222 conductors are on two separate layers of integration (e.g. using dual layers of metallization). This allows more flexibility in laying out the conduction paths 220, 222 for the supply current (i_s) and return current (i_R). Supply current i_s drawn by the IC 114a from the power supply VDD flows through the active chip areas 214 as circuit current i_C and then flows back (e.g. to circuit ground GND) as return current i_R.

As is well known in the art, this current flow causes electromagnetic fields to be generated, the fields of primary interest being those resulting from the flow of the supply i_s and return i_R currents (due to these currents' concentration along their integrated conduction paths 220, 222). However, due to the directions of flow of these currents i_s, i_R, the electromagnetic fields caused by these currents i_s, i_R, being substantially equal and of substantially opposite polarity, will tend to cancel each other out.

This field cancellation is further enhanced by the fact that the current loops formed by the integrated conduction paths 220, 222 and active chip areas 214 are substantially symmetrical and coplanar. (The symmetry of the current loops are evident from the figure, and, as should be understood, the current loops formed are substantially coplanar since the vertical separation(s) of the integrated conduction paths 220, 222 and active chip areas 214 is(are) very small.)

Referring to Figure 4, an IC design 114b suitable for the packaged IC 110 of Figure 2A with power supply and ground connections at two opposing edges of the package 112 can have integrated power supply VDD 220 and ground GND 222 conductors configured as shown. With this IC 114b configuration, an additional power supply VDD conductor 124a is connected via a bond wire 124b to the other power supply VDD connector 124. Additional ground GND conductors 126a are connected via bond wires 126b to the other ground connectors 126.

As with the IC design 114a of Figure 3, the current loops formed by the integrated conduction paths 220, 222 and active chip areas 214 are substantially symmetrical and coplanar. Therefore, the electromagnetic fields caused by the supply i_s and return i_R currents, being substantially equal and of substantially opposite polarity, will tend to cancel each other out.

Referring to Figure 5, an IC design 114c also suitable for the packaged IC 110 of Figure 2A with power supply and ground connections along one edge can have integrated power supply VDD 220 and ground GND 222 conductors configured as shown. In this IC design 114c, the power supply VDD 220 and ground GND 222 conductors are on the same integration layer (e.g. single layer of metallization). While this generally allows less flexibility in laying out the conduction paths 220, 222 for the supply i_s and return i_R currents, it may nonetheless be desireable for avoiding an otherwise unnecessary integration layer.

As with the IC design 114a of Figure 3, the current loops formed by the integrated conduction paths 220, 222 and active chip areas 214 are substantially symmetrical and coplanar. But, due to the use of only one integration layer for the supply 220 and return 222 current paths, the current loops formed differ from those in the IC design 114a of Figure 3. For example, within the interior of the IC 114c, the supply i_s and return i_R currents flow in the same general directions, and therefore, produce electromagnetic fields which tend to sum together. However, near the periphery of the IC 114c, the return currents i_R (the sum of which now equals the total supply current i_s provided by the power supply VDD) produce electromagnetic fields which tend to sum together and cancel those produced within the interior.

Referring to Figure 6, an IC design 114d suitable for the packaged IC 110 of Figure 2A with power supply and ground connections at two opposing edges of the package 112 can have integrated power supply VDD 220 and ground GND 222 conductors configured as shown. With this IC 114d configuration, an additional power supply VDD conductor 124a is connected via a bond wire 124b to the other power supply VDD connector 124. Additional ground GND conductors 126a are connected via bond wires 126b to the other ground connectors 126.

As with the IC design 114b of Figure 4, the current loops formed by the integrated conduction paths 220, 222 and active chip areas 214 are substantially symmetrical and coplanar. But, due to the use of only one integration layer for the supply 220 and return 222 current paths, the current loops formed differ from those in the IC design 114b of Figure 4. For example, within some portions of the interior of the IC 114d, the supply i_s and return i_R currents flow in the same general directions, and therefore, produce electromagnetic fields which tend to sum together. However, within other portions of the interior and near the periphery of the IC 114d, the return currents i_R produce electromagnetic fields which tend to sum together and cancel those produced elsewhere within the interior.

It should be understood that the power supply VDD and ground GND connections shown in Figures 3 through 6 can be reversed to be configured in accordance with Figures 1B and 2B (with a ground GND connection between two power supply VDD connections). Such a configuration of power supply VDD and ground GND connections would, in accordance with the foregoing discussion, provide similar advantages and benefits of substantially self-cancelling electromagnetic fields produced by on-board supply i_s and return i_R currents.

Various other modifications and alterations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and spirit of this invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments.

WHAT IS CLAIMED IS:

1. A packaged integrated circuit with reduced radiation of and susceptibility to electromagnetic fields, comprising:

an integrated circuit package which includes first and second opposing edges;

an integrated circuit, within said integrated circuit package, which includes a plurality of power supply conductors, a plurality of ground conductors, and first and second pluralities of signal conductors, wherein said plurality of power supply conductors form a supply current loop and said plurality of ground conductors form a return current loop, and wherein said supply and return current loops are substantially symmetrical and coplanar;

a first plurality of signal connectors disposed along said first integrated circuit package edge and connected to said first plurality of integrated circuit signal conductors;

a first single power supply connector disposed among said first plurality of signal connectors and connected to said plurality of integrated circuit power supply conductors; and

a first plurality of ground connectors disposed among said first plurality of signal connectors on opposing sides of said first single power supply connector and connected to said plurality of integrated circuit ground conductors.

2. A packaged integrated circuit as recited in Claim 1, wherein said supply current loop has a supply loop area associated therewith, said return current loop has a return loop area associated therewith, said supply and return current loops are tangent to one another, and said supply and return loop areas are approximately equal.

3. A packaged integrated circuit as recited in Claim 1, wherein said first plurality of signal connectors, said first single power supply connector and said first plurality of ground connectors comprise a plurality of metal pins.

4. A packaged integrated circuit as recited in Claim 1, wherein said first single power supply connector and said first plurality of ground connectors are linearly disposed along said first integrated circuit package edge with equidistant adjacent connector centers.

5. A packaged integrated circuit as recited in Claim 1, further comprising:

a second plurality of signal connectors disposed along said second integrated circuit package edge and connected to said second plurality of integrated circuit signal conductors;

a second single power supply connector disposed among said second plurality of signal connectors and connected to said plurality of integrated circuit power supply conductors; and

a second plurality of ground connectors disposed among said second plurality of signal connectors on opposing sides of said second single power supply connector and connected to said plurality of integrated circuit ground conductors.

6. A packaged integrated circuit as recited in Claim 5, wherein said first and second pluralities of signal connectors, said first and second single power supply connectors, and said first and second pluralities of ground connectors comprise a plurality of metal pins.

7. A packaged integrated circuit as recited in Claim 5, wherein said first single power supply connector and said first plurality of ground connectors are linearly disposed along said first integrated circuit package edge with first equidistant adjacent connector centers, and said second single power supply

connector and said second plurality of ground connectors are linearly disposed along said second integrated circuit package edge with second equidistant adjacent connector centers.

8. A packaged integrated circuit as recited in Claim 1, further comprising:

a second plurality of signal connectors disposed along said second integrated circuit package edge and connected to said second plurality of integrated circuit signal conductors;

a first single ground connector disposed among said second plurality of signal connectors and connected to said plurality of integrated circuit ground conductors; and

a first plurality of power supply connectors disposed among said second plurality of signal connectors on opposing sides of said first single ground connector and connected to said plurality of integrated circuit power supply conductors.

9. A packaged integrated circuit as recited in Claim 8, wherein said first and second pluralities of signal connectors, said first single power supply connector, said first plurality of ground connectors, said first single ground connector and said first plurality of power supply connectors comprise a plurality of metal pins.

10. A packaged integrated circuit as recited in Claim 8, wherein said first single power supply connector and said first plurality of ground connectors are linearly disposed along said first integrated circuit package edge with first equidistant adjacent connector centers, and said first single ground connector and said first plurality of power supply connectors are linearly disposed along said second integrated circuit package edge with second equidistant adjacent connector centers.

11. A packaged integrated circuit with reduced radiation of and susceptibility to electromagnetic fields, comprising:

an integrated circuit package which includes first and second opposing edges;

an integrated circuit, within said integrated circuit package, which includes a plurality of power supply conductors, a plurality of ground conductors, and first and second pluralities of signal conductors, wherein said plurality of power supply conductors form a supply current loop and said plurality of ground conductors form a return current loop, and wherein said supply and return current loops are substantially symmetrical and coplanar;

a first plurality of signal connectors disposed along said first integrated circuit package edge and connected to said first plurality of integrated circuit signal conductors;

a first ground connector disposed among said first plurality of signal connectors and connected to said plurality of integrated circuit ground conductors; and

a first plurality of power supply connectors disposed among said first plurality of signal connectors on opposing sides of said first ground connector and connected to said plurality of integrated circuit power supply conductors.

12. A packaged integrated circuit as recited in Claim 11, wherein said supply current loop has a supply loop area associated therewith, said return current loop has a return loop area associated therewith, said supply and return current loops are tangent to one another, and said supply and return loop areas are approximately equal.

13. A packaged integrated circuit as recited in Claim 11, wherein said first plurality of signal connectors, said first ground connector and said first plurality of power supply connectors comprise a plurality of metal pins.

14. A packaged integrated circuit as recited in Claim 11, wherein said first ground connector and said first plurality of power supply connectors are linearly disposed along said first integrated circuit package edge with equidistant adjacent connector centers.

15. A packaged integrated circuit as recited in Claim 11, further comprising:

a second plurality of signal connectors disposed along said second integrated circuit package edge and connected to said second plurality of integrated circuit signal conductors;

a second ground connector disposed among said second plurality of signal connectors and connected to said plurality of integrated circuit ground conductors; and

a second plurality of power supply connectors disposed among said second plurality of signal connectors on opposing sides of said second ground connector and connected to said plurality of integrated circuit power supply conductors.

16. A packaged integrated circuit as recited in Claim 15, wherein said first and second pluralities of signal connectors, said first and second ground connectors, and said first and second pluralities of power supply connectors comprise a plurality of metal pins.

17. A packaged integrated circuit as recited in Claim 15, wherein said first ground connector and said first plurality of power supply connectors are linearly disposed along said first integrated circuit package edge with first equidistant adjacent connector centers, and said second ground connector and said second plurality of power supply connectors are linearly disposed along said second integrated circuit package edge with second equidistant adjacent connector centers.

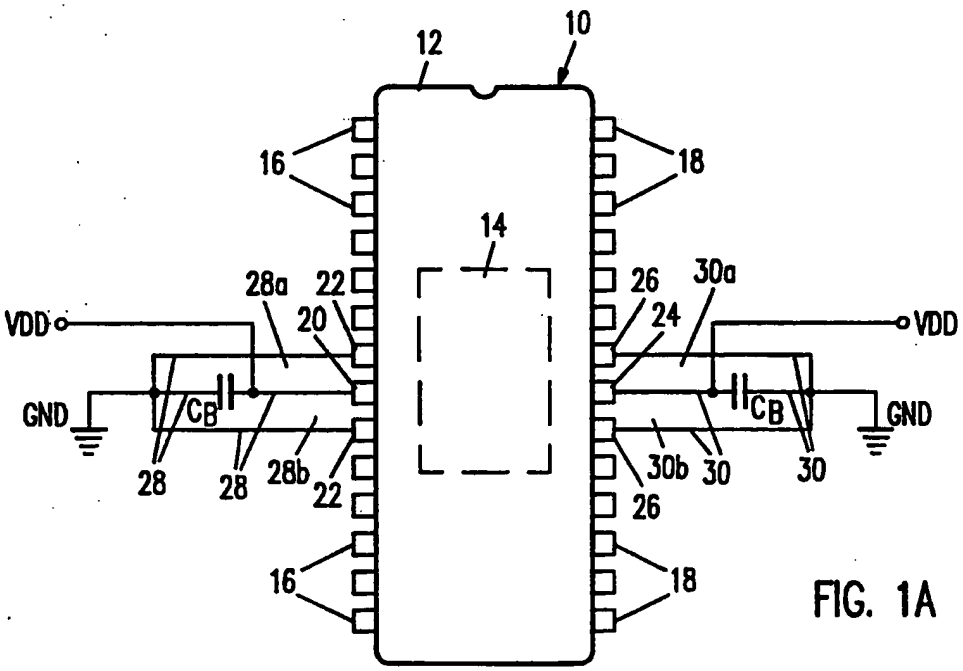


FIG. 1A

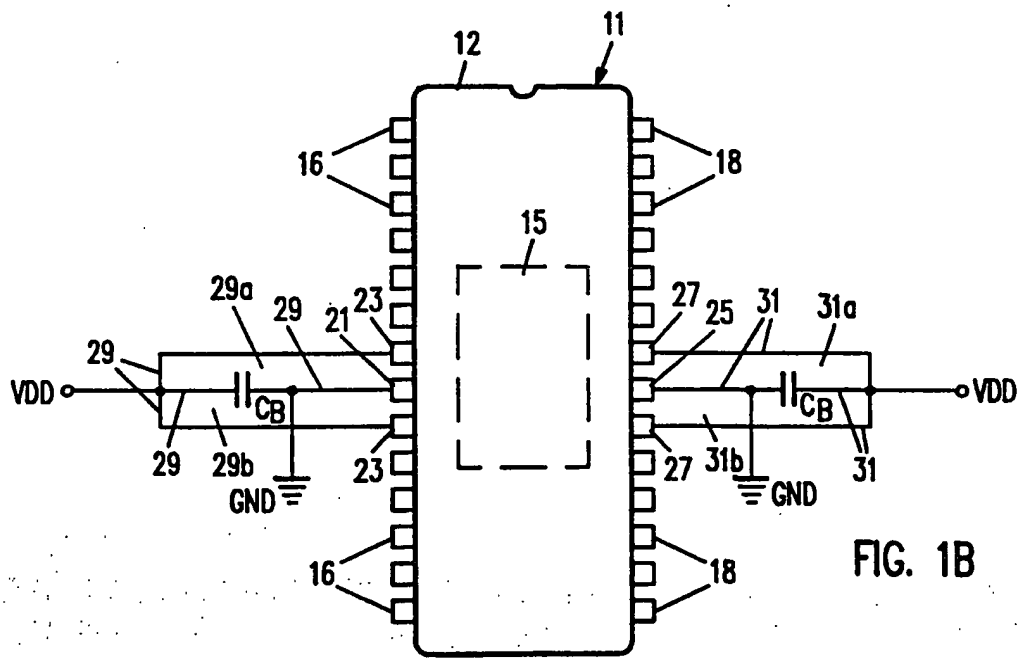


FIG. 1B

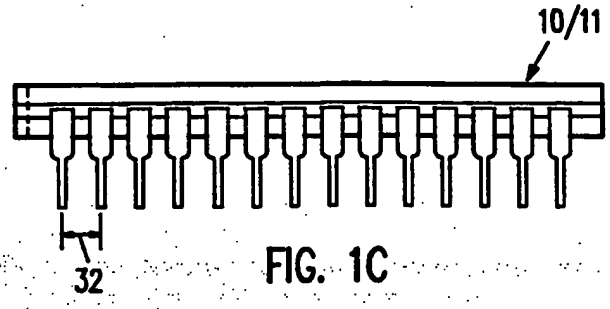
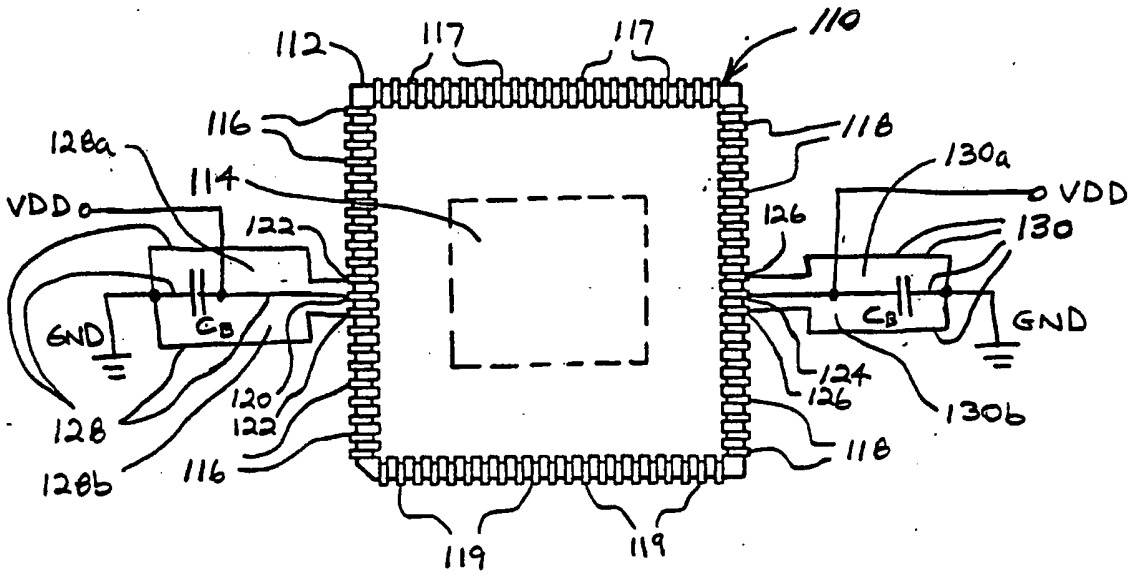


FIG. 1C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VDD
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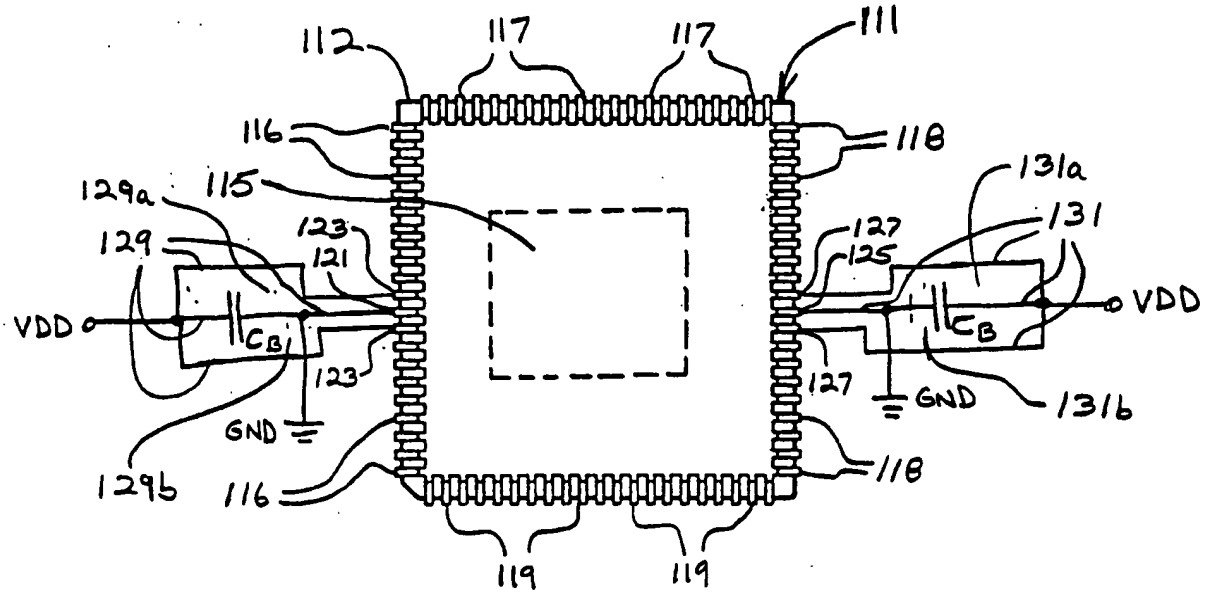
126
120
122
128
130b
128b
116
118
119
119

(A)

FIGURE 2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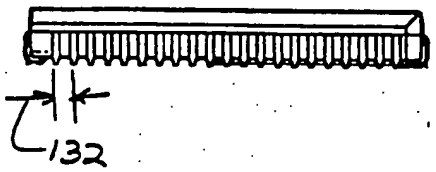
(B)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(C)

FIGURE 2

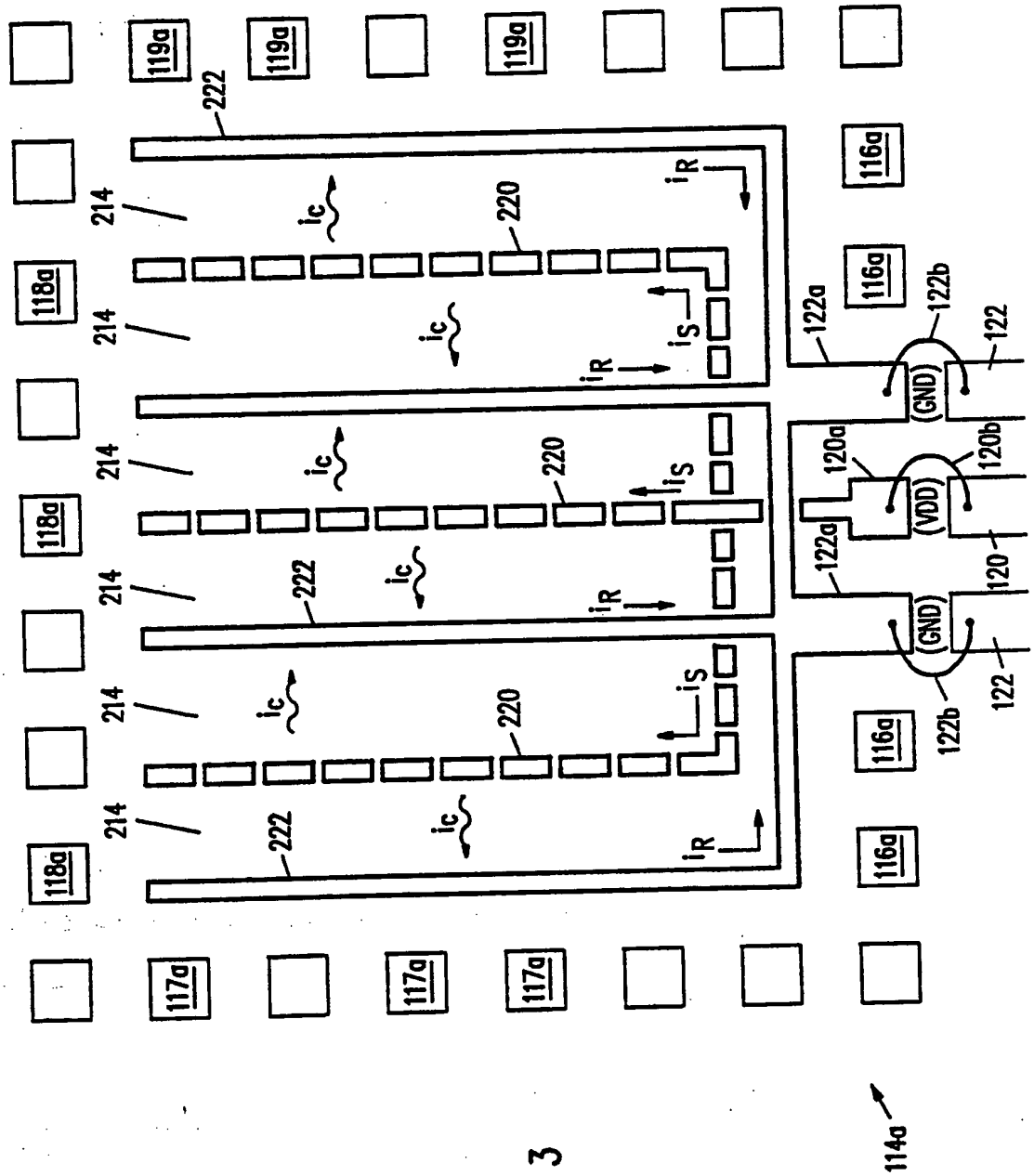
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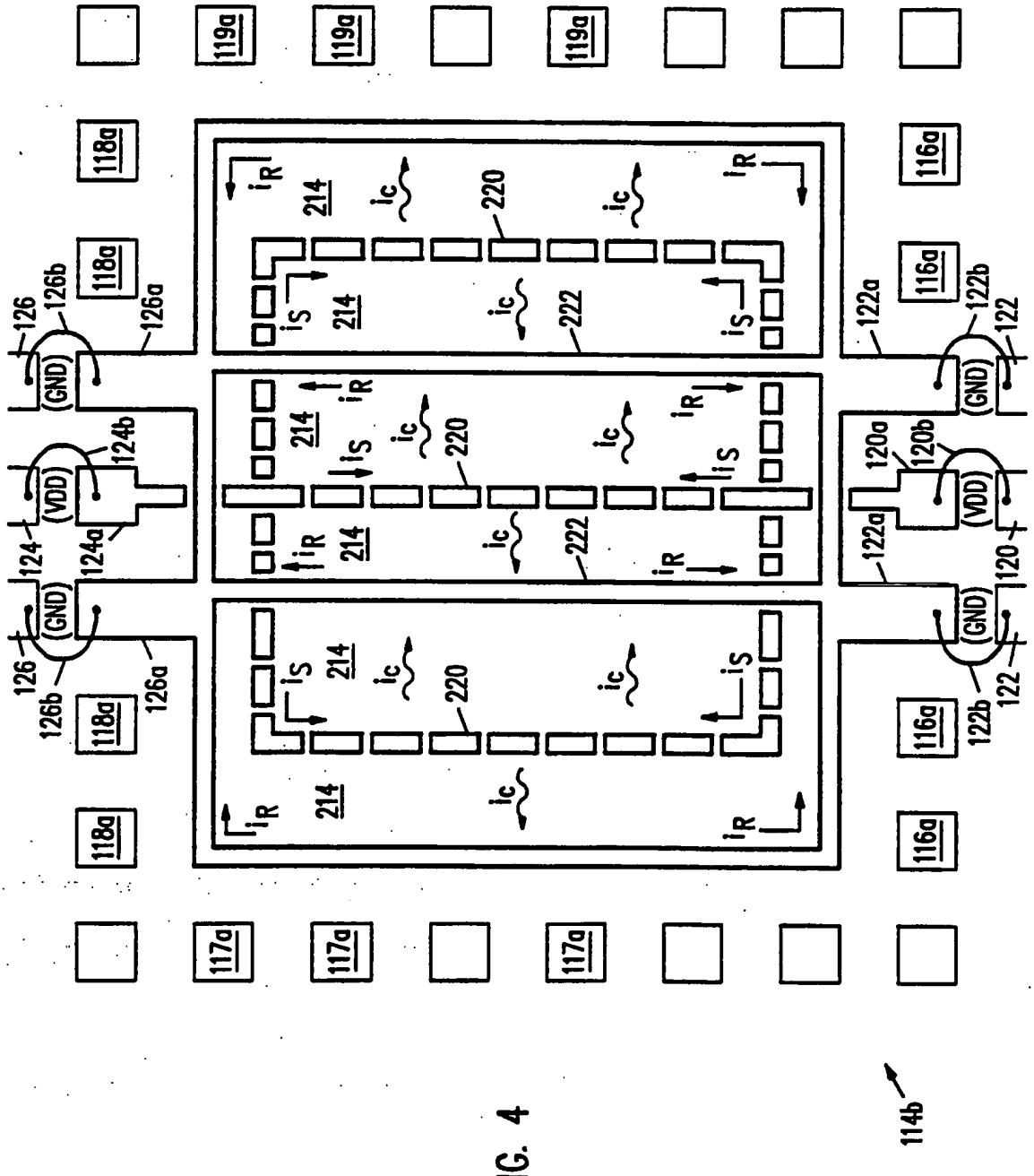
FIG. 3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120b
120
214
220
222
i_R
i_S
i_C
117a
114b

FIG. 4

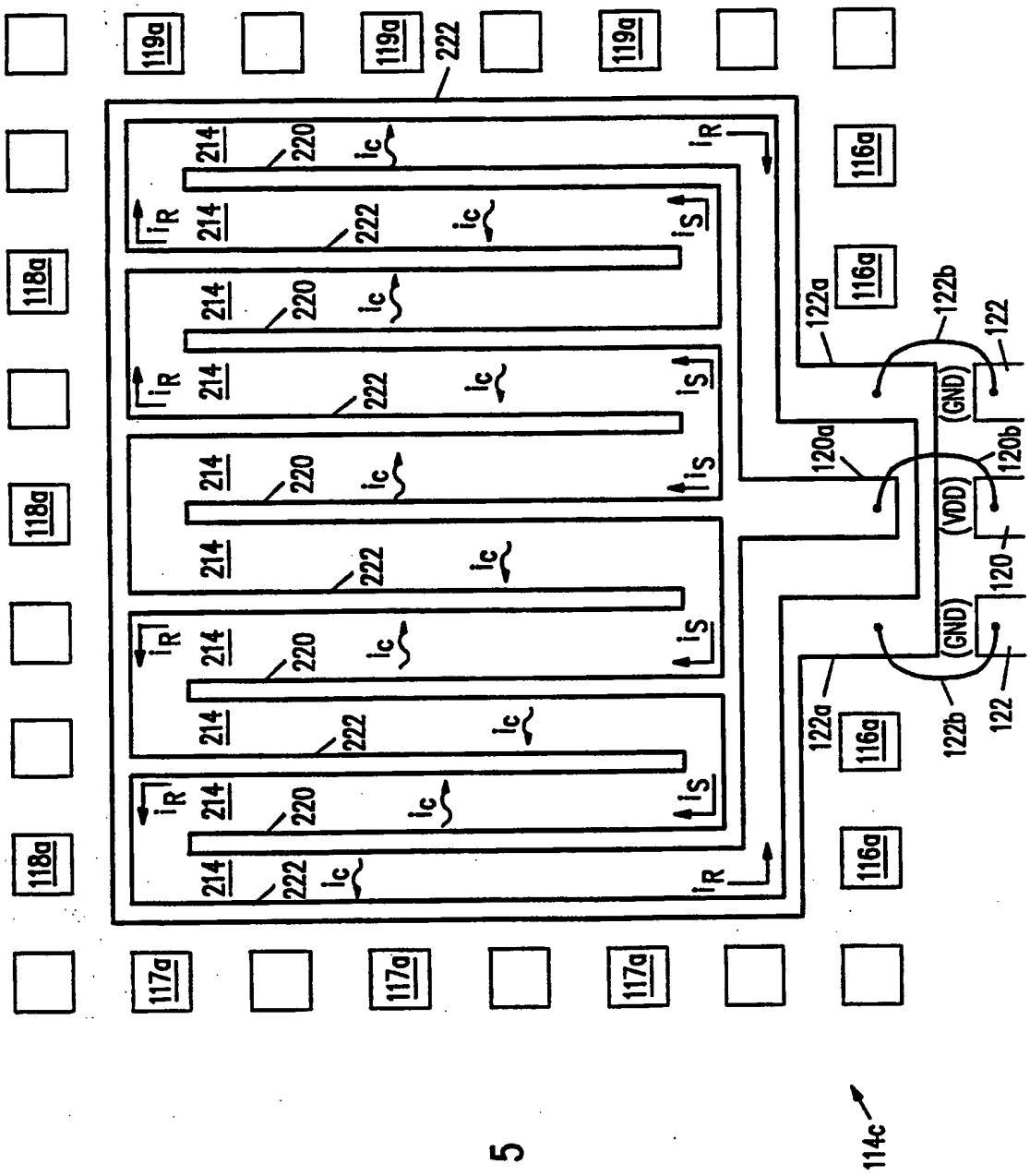
119a
222
214
220
i_c
i_R
i_S
116a
118a
117a
122a
122b
122
(GND)
120a
120b
(VDD)
120
114c

FIG. 5

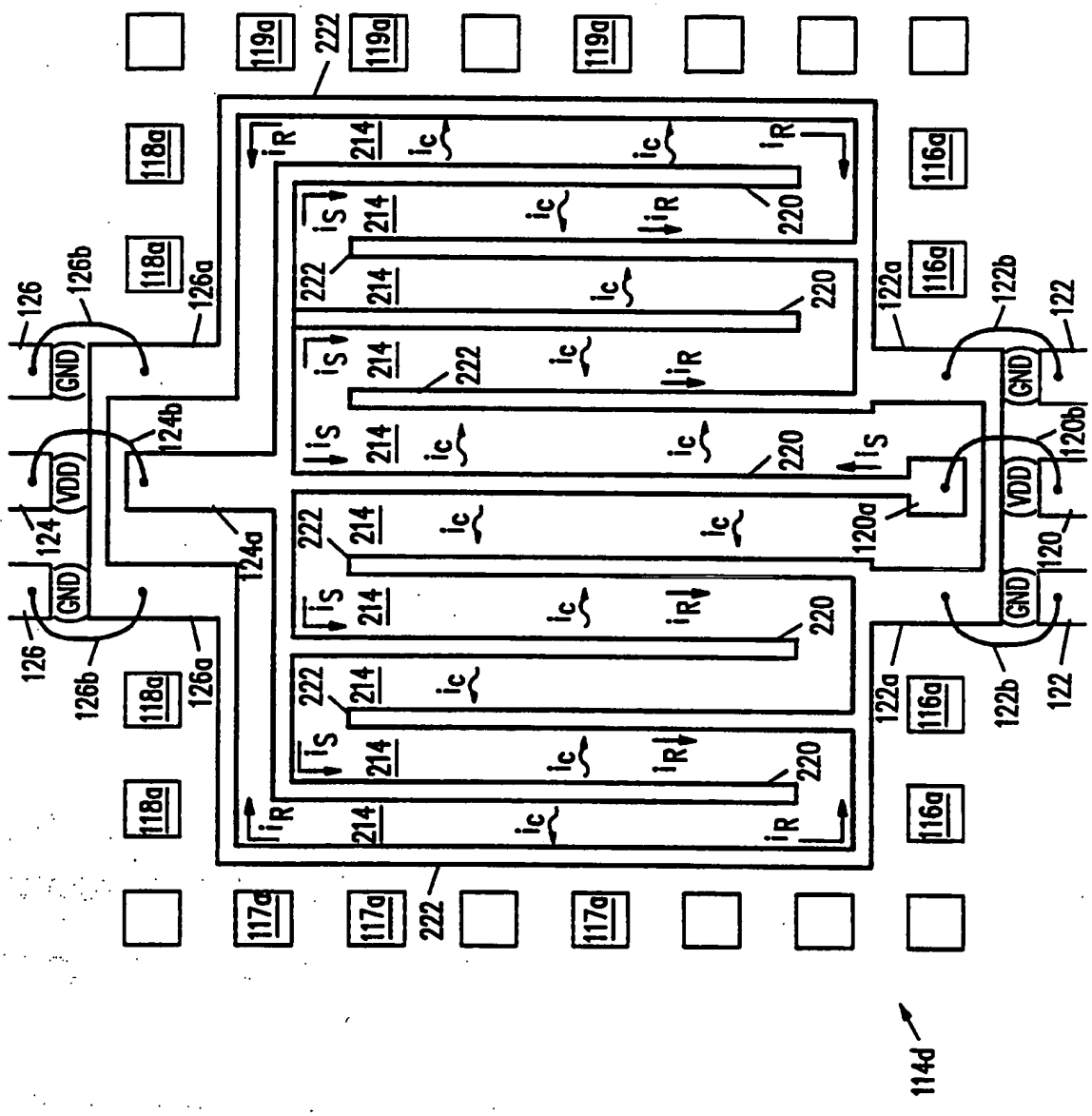
119a
222
118a
116a
214
220
126
126b
126a
122a
122b
122
GND
VDD
124b
120b
124
124a
120a
120
117a
114d

FIG. 6

INTERNATIONAL SEARCH REPORT

Intern[illegible]l Application No
PCT/US 94/08115

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/552 H01L23/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 11, no. 152 (E-507) 16 May 1987 & JP,A,61 288 451 (TOSHIBA) 18 December 1986 see abstract	1
A	EP,A,0 382 948 (PHILIPS) 22 August 1990 see column 2, line 37 - line 52	1
A	EP,A,0 354 371 (SANYO) 14 February 1990	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
28 December 1994	16. 01. 95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	De Raeve, R

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INTERNATIONAL SEARCH REPORT

information on patent family members

Intern. al Application No
PCT/US 94/08115

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
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		JP-A-	2277262	13-11-90
		US-A-	5126822	30-06-92
EP-A-0354371	14-02-90	JP-A-	2023634	25-01-90
		JP-B-	6052771	06-07-94
		JP-A-	2051272	21-02-90
		JP-A-	2137245	25-05-90
		DE-D-	68915072	09-06-94
		DE-T-	68915072	08-12-94
		US-A-	5050238	17-09-91
		US-A-	5111274	05-05-92